

CLAIMS

What is claimed is:

1. A microphone bias circuit for use within an integrated circuit having a microphone input, the microphone bias circuit comprises:

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a first integrated circuit (IC) pin;

a first resistor operably coupled to the first IC pin and a return voltage;

10 a second IC pin operably coupled to receive analog signals from a microphone; and

a variable supply voltage buffer operably coupled to produce a buffered supply voltage based on a variable impedance setting, wherein at least one off-chip component couples the second IC pin to the first IC pin and wherein the variable supply voltage buffer provides the buffered supply voltage to second IC pin as a microphone bias voltage.

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2. The microphone bias circuit of claim 1, wherein the power supply buffer comprises:

20 an amplifier having a first input, a second input, and an output, wherein the first input is coupled to receive a bandgap voltage and the output provides the buffered supply voltage; and

a variable impedance having a first node, a second node, and a tap node, wherein the first node is coupled to the output of the amplifier, the second node is coupled to the return voltage, and the tap node is coupled to the second input of the amplifier.

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3. The microphone bias circuit of claim 2, wherein the variable impedance comprises an on-chip variable resistor circuit.

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4. The microphone bias circuit of claim 1, wherein the at least one off-chip component comprises a capacitor.

5. The microphone bias circuit of claim 1 further comprises:

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a second resistor coupled between the variable supply voltage buffer and the second IC pin.

6. The microphone bias circuit of claim 1 further comprises:

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a processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

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monitor the received analog signals;

determine whether the received analog signals are optimally biased; and

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when the received analog signals are not optimally biased, adjust the variable supply voltage buffer to optimally bias the received analog signals.

7. The microphone bias circuit of claim 1, wherein the supply voltage buffer comprises:

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a power down input operably coupled to receive a power down signal, wherein, when the power down signal is in a first state, the supply voltage buffer is enabled and when the power down signal is in a second state, the supply voltage buffer is disabled.

8. An integrated circuit for use in a multiple function handheld device, the integrated circuit comprises:

5 a processing module operably coupled to perform at least one algorithm relating to a function of the multiple function handheld device;

10 an analog to digital converter operably coupled to convert analog signals into digital signals, wherein the digital signals are processed by the processing module while performing the at least one algorithm;

a microphone input circuit operably coupled to provide the analog signals to the analog to digital converter, wherein the microphone input circuit includes:

15 an amplifier operably coupled to amplify received input analog signals to produce the analog signals; and

a microphone bias circuit that includes:

20 a first integrated circuit (IC) pin;

a first resistor operably coupled to the first IC pin and a return voltage;

25 a second IC pin operably coupled to receive analog signals from a microphone; and

30 a variable supply voltage buffer operably coupled to produce a buffered supply voltage based on a variable impedance setting, wherein at least one off-chip component couples the second IC pin to the first IC pin and wherein the variable supply voltage buffer provides the buffered supply voltage to second IC pin as a microphone bias voltage.

9. The integrated circuit of claim 8, wherein the power supply buffer comprises:

an amplifier having a first input, a second input, and an output, wherein the first input is coupled to receive a bandgap voltage and the output provides the buffered supply
5 voltage; and

a variable impedance having a first node, a second node, and a tap node, wherein the first node is coupled to the output of the amplifier, the second node is coupled to the return voltage, and the tap node is coupled to the second input of the amplifier.

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10. The integrated circuit of claim 9, wherein the variable impedance comprises an on-chip variable resistor circuit.

11. The integrated circuit of claim 8, wherein the at least one off-chip component
15 comprises a capacitor.

12. The integrated circuit of claim 8, wherein the microphone bias circuit further comprises:

20 a second resistor coupled between the variable supply voltage buffer and the second IC pin.

13. The integrated circuit of claim 8, wherein the processing module further functions to:

25 monitor the received analog signals;

determine whether the received analog signals are optimally biased; and

when the received analog signals are not optimally biased, adjust the variable supply
30 voltage buffer to optimally bias the received analog signals.

14. The integrated circuit of claim 8, wherein the supply voltage buffer comprises:

a power down input operably coupled to receive a power down signal, wherein, when the power down signal is in a first state, the supply voltage buffer is enabled and when the

5 power down signal is in a second state, the supply voltage buffer is disabled.